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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/385,666	08/26/1999	ROBERTO SUAYA	002282.P066	9500

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EXAMINER	
PHAN, THAI Q	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 08/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/385,666	SUAYA ET AL.	
	Examiner	Art Unit	
	Thai Q. Phan	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *51-57* is/are allowed.

6)☒ Claim(s) *15-31 and 33-50* is/are rejected.

7)☒ Claim(s) *32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 February 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892) ✓
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to applicant's amendment filed on 05/03/2004. Claims 15-57 are now pending in the Action.

Drawings

Formal drawings are acceptable for examination.

Information Disclosure Statement

The information disclosure statement filed 02/19/2003 has been considered.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 15-31 and 33-50 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen, James by 6,300,765 B1.

As per claim 15, Chen anticipates a method and system for measuring cross-coupling capacitances in an integrated circuits with feature limitations as claimed

(Abstract and Summary of the Invention). According to Chen, the measurement method includes steps

Providing at least first and second wires in a wire interconnection structure (col. 3, lines 10-28), charging interconnect wiring to a predetermined voltage by charging means (col. 3, lines 51-63),

Performing a first measurement associated with a capacitance of the first wire (col. 5, lines 33-45),

Charging the second wire to the predetermined voltage, discharging (recharging) the first wire to the predetermined voltage, performing a second measurement associated with a capacitance of the first wire, and calculating a charge difference due to charge induced between the first and second measurement for induced charge on the target interconnect to determine the cross-coupling capacitance between the first and second wire by control voltage (Background of the Invention, col. 5, line 5 to col. 7, line 33). The induced charge on the test interconnect during the measurement above is the charge difference as claimed. Such charge difference is due to charge induced on the measured wire during measurement.

As per claim 16, Chen anticipates coupling series transistor with configuration as claimed (Fig. 1).

As per claim 17, Chen further anticipates step of applying periodic signals to the transistor gates as claimed (Fig. 1).

As per claim 18, Chen discloses the applied signals are periodic and synchronous or not simultaneous (Fig 3, col. 5, line 33 to col. 6, line 55).

As per claim 19, Chen discloses charging and discharging interconnection wires in order.

As per claim 20, Chen discloses measuring cross-coupling capacitances for multiple wire interconnections (Figs. 1-3, cols. 5 and 6).

As per claims 21-22, Chen discloses means for measuring cross coupling capacitances for multiple neighbor wires and using the same measurement techniques for wire neighbor.

As per claim 23, Chen uses transistors in conjunction with transmission wire for measurement.

As per claims 24-25, Chen anticipates capacitance measurement for wires in multilayer integrated circuit, repeating the measurement over a number of cycle over a timing diagram to compute a correct measurement (cols. 5-6).

As per claims 26 and 27, Chen discloses measuring charge and current for capacitance measurement.

As per claims 28-31, Chen discloses logic inverter connected between transmission wires for the test interconnect charging circuit (Fig. 1, block (117)).

As per claims 33-34, Chen anticipates transistor in conjunction with transmission wires and effect of neighbor wires in capacitance measure.

As per claim 35, Chen anticipates method and system for measuring cross-coupling capacitances in an integrated circuits with feature limitations as claimed (Summary of the Invention). According to Chen, the measurement method includes means for providing a first and second transistors coupled in series (Fig. 1), means for

providing at least first and second wires in a wire interconnection structure (col. 3, lines 10-30), charging interconnect wires to a predetermined voltage by charging means (col. 3, lines 59-65), performing a first measurement associated with a capacitance of the first wire (col. 5, lines 35-59), charging the second wire to the predetermined voltage, discharging or recharging the charged first wire to the predetermined voltage, performing a second measurement associated with a capacitance of the first wire, and calculating a difference between the first and second measurement (subtraction) due to charge induced or relative charge induced on the target interconnect to determine the cross-coupling capacitance between the first and second wire as claimed (Background of the Invention, col. 5, line 5 to col. 7, line 33).

As per claim 36, Chen anticipates low/high logic values feature as claimed.

As per claims 37-38, Chen anticipates a logic coupled to the interconnection wires such logic including inverter, gates, etc. as claimed (Figs. 1-3).

As per claims 39-41, Chen anticipates the claimed limitations for measurement of cross-coupling capacitance. Such features include a plurality of periodic signals are used to control charging the first wire and periodic signal is used to control the charging of the second wire (Fig. 3).

As per claim 42, Chen anticipates ammeter for measuring cross-coupling capacitances.

As per claim 43, Chen anticipates measurement of cross-coupling capacitance for multiple neighbor wires to the first wire.

As per claim 44, Chen anticipates means for measuring cross coupling capacitances for multiple neighbor wires and using the same measurement techniques for wire neighbor.

As per claims 45-46, Chen anticipates capacitance measurement for wires in multilayer integrated circuit, repeating the measurement over a number of cycle over a timing diagram to compute a correct measurement and the measurement is accomplished with library element or with measurement tools (cols. 5-6).

As per claim 47, Chen anticipates a method and system for measuring cross-coupling capacitances in an integrated circuits with feature limitations as claimed (Summary of the Invention). According to Chen, the measurement method includes means for providing a first and second transistors coupled in series (Fig. 1), means for providing at least first and second wires in a wire interconnection structure (col. 3, lines 10-30), charging interconnect wiring to a predetermined voltage by charging means (col. 3, lines 59-65), performing a first measurement associated with a capacitance of the first wire (col. 5, lines 3559), charging the second wire to the predetermined voltage, discharging or recharging the charged first wire to the predetermined voltage, usually at lower voltage level, performing a second measurement associated with a capacitance of the first wire, and calculating a charge difference or relative charge induced on the target interconnect (col. 6, lines 22-56, for example) between the first and second measurement to determine the cross-coupling capacitance of the interconnect wires claimed (Background of the Invention, col. 5, line 5 to col. 7, line 33).

As per claims 48-50, Chen anticipates such feature limitations for cross-coupling capacitance measurement.

Allowable Subject Matter

1. Claims 51-57 are allowable over the prior art of record. The following is a statement of reasons for the indication of allowable subject matter:

2. Claims 51-57 are directed to a method for determining cross-coupling capacitance of an interconnect target. The method of measurement cross-coupling capacitance includes steps applying a third periodic signal to charge and discharge a second wire that is in cross-coupling relationship with the first wire, measuring a first charge that is deposited on the first wire over the period of time, the first charge being measured each time the second wire is grounded, measuring a second charge that is deposited on the first wire over the period of time, the second charge being measured each time the second wire is charged to the supply voltage, and calculating a different between the first and second charge to determine the cross-coupling capacitance as claimed. The closest prior art of record does not expressly disclose or suggest the method of measurement of charge coupling capacitance by referencing charge difference deposited on the target wire for the step of applying the third periodic signal to charge and discharge the second wire that is in cross-coupling relationship with the first wire.

3. Claim 32 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 32 further requires measure step (e) of during the second period of time, applying the first periodic signal to the gate of the first transistor and the second periodic signal to the gate of the second transistor to charge and discharge the first wire, wherein the first and second transistor are not activated simultaneously, and step (f) repeatedly performing the second measurement during the second period of time and averaging a result of the second measurement as claimed. Because Chen does not expressly disclose the present test pattern as claimed, claim 32 is objected to as being dependent of the rejected base claim.

Response to Arguments

Applicant's arguments filed 05/03/2004 have been fully considered but they are not persuasive.

In response to applicant's argument Chen does not anticipate or suggest "charge difference being calculated between first and second measurement to determine cross-coupling capacitance" on pages 11 and 12, the examiner disagrees with. Chen anticipates charge induced or charge difference between the first and second measurement. Such charge difference due to charge induced on the target interconnect is used to determine the cross-coupling capacitance between the first and second wire by control voltage (Background of the Invention, col. 5, line 5 to col. 7, line

33). The induced charge on the test interconnect during the measurement above is the charge difference as claimed.

Conclusion

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Q. Phan whose telephone number is 703-305-3812. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached on 703-308-6647. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

3. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aug. 20, 2004

Thai Phan
Patent Examiner
AU: 2128